Curriculum Vitae

Lyl Mercedes CIGANDA BRASCA

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Sistema Nacional de Investigadores

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información

Categorización actual: Iniciación

Ingreso al SNI: Iniciación (01/06/2015)

Datos generales

Información de contacto

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Dirección: Manuel Otero 6354, CP. 11500, Montevideo, Uruguay

Institución principal

Instituto de Ingeniería Eléctrica / Facultad de Ingeniería - UDeLaR / Universidad de la República / Uruguay

Dirección institucional

Dirección: Facultad de Ingeniería - UDeLaR / Julio Herrera y Reissig 565 / 11300 / Montevideo / Montevideo / Uruguay

Teléfono: (+00598) 27110974

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Formación

Formación concluida

Formación académica/Titulación

Posgrado

2010 - 2013

Doctorado

Computer and Control Engineering

Politecnico di Torino , Italia

Título: New Techniques for Reliability Characterization of Electronic Circuits

Tutor/es: Paolo Bernardi

Obtención del título: 2013

Becario de: Politecnico di Torino , Italia

Sitio web de la Tesis: http://porto.polito.it/id/eprint/2507391

Palabras clave: reliability characterization; integrated circuit testing; software-based self-test; digital logic design; microprocessor

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal

Grado

1998 - 2004 Grado

Ingeniería Eléctrica

Facultad de Ingeniería - UDeLaR, Universidad de la República , Uruguay

Título: FitoInc. Un incubador para plantas.

Tutor/es: Enrique Ferreira

Obtención del título: 2004

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Sistemas de Automatización y Control / Control de temperatura

Construcción institucional

Idiomas

Español

Entiende (Muy Bien) / Habla (Muy Bien) / Lee (Muy Bien) / Escribe (Muy Bien)

Francés

Entiende (Regular) / Habla (Regular) / Lee (Regular) / Escribe (Regular)

Inglés

Entiende (Muy Bien) / Habla (Muy Bien) / Lee (Muy Bien) / Escribe (Muy Bien)

Italiano

Entiende (Muy Bien) / Habla (Muy Bien) / Lee (Muy Bien) / Escribe (Bien)

Areas de actuación

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Hardware y Arquitectura de Computadoras

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Telecomunicaciones

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Education

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / diseño de circuitos digitales

Actuación Profesional

Cargos desempeñados actualmente

Desde: 12/2008

6869 , (Docente Grado 2 Titular, 6 horas semanales) , Facultad de Ingeniería - UDeLaR , Uruguay

Desde: 03/2015

Ingeniero Eléctrico Nivel B , (40 horas semanales) , Administración Nacional de Telecomunicaciones , Uruguay

Universidad de la República , Facultad de Ingeniería - UDeLaR , Uruguay

Vínculos con la institución

12/2008 - Actual, Vínculo: 6869, Docente Grado 2 Titular, (6 horas semanales)

04/2004 - 12/2008, *Vínculo:* , Docente Grado 1 Interino, (20 horas semanales)

Politecnico di Torino , Italia

Vínculos con la institución

01/2010 - 12/2012, *Vínculo:* PhD Student, (50 horas semanales / Dedicación total)

01/2013 - 06/2013, *Vínculo:* Research Fellow , (50 horas semanales / Dedicación total)

07/2013 - 12/2014, Vínculo: Post Doc Research Fellow, (50 horas semanales / Dedicación total)

Actividades

03/2010 - 12/2014

Docencia , Grado

Informática (Lenguaje C) , Asistente , Computer and Control Engineering

Institut National Polytechnique de Grenoble , Institut National Polytechnique de Grenoble , Francia

Vínculos con la institución

09/2012 - 01/2013, *Vínculo:* Visitante, (50 horas semanales / Dedicación total)

Empresa Pública , Administración Nacional de Telecomunicaciones , Uruguay

Vínculos con la institución

11/2001 - 05/2005, *Vínculo:* Becario Estudiante de Ingenieria, (30 horas semanales)

05/2005 - 01/2010, *Vínculo:* Ingeniro Civil/Electrico, (40 horas semanales)

03/2015 - Actual, Vínculo: Ingeniero Eléctrico Nivel B, (40 horas semanales)

Producción científica/tecnológica

My work falls in the low cost testing domain. Strategies for new and/or improved SBST, DfT and ATE mechanisms are proposed, implemented and evaluated. The strategies deal mainly with memories, processor and mixed-signal devices (analogue-to-digital converters is our target device) embedded in Systems-on-a-Chip, where standard communication protocols and wrappers are used to communicate with the device under test. Integrated electronic systems are increasingly used in an wide number of applications and environments, ranging from critical missions to low cost consumer products. However, there are many difficult challenges associated with continued cost reduction, size reduction, improved performance and improved power efficiency. One of these challenges is the reliability of these electronic systems. Manufacturing processes, intrinsic aging phenomena of components and environmental stress may cause internal defects and damages during the lifetime of a system, possibly causing misbehaviours or failures. In order to guarantee product quality and consumer satisfaction, it is necessary not only to discover faults as soon as possible in the manufacturing process, but also to continuously check for their absence throughout a product lifetime. With testers being expensive pieces of equipment and the cost of transistors continuously decreasing, it makes sense to use some of these low-cost transistors to replace the costly test tools, whenever possible. The first low cost approach we can think about is using the devices themselves to implement their own test. This is the underlying motivation of functional Software-Based Self-Test (SBST): a fast, powerful microprocessor, which has lots of resources, could certainty help in its testing procedure. Having the advantages of enabling at-speed testing, zero area overhead and actually testing the device's operation, this approach also has some drawbacks. Even if SBST is essentially suitable for online testing (and sometimes it is the only possible approach), it requires some dedicated system memory for the functional testing data, which can reach very big sizes. Also some faults happen to be functionally untestable. A second approach to low cost testing is design for test (DfT). Add some extra (cheap) area on-chip specifically in charge of performing tests. The DfT path started long ago, but it is still a key element in 2013 International Technology Roadmap for Semiconductors test roadmap. Logic and Memory Built-In Self Test schemas are usual practises. Analogue DfT is also an interesting strategy, especially when the analogue or mixed-signal device is integrated in a wider digital system like a SoC. Finally, there are some fields where the use of external (and generally expensive) testers is mandatory. Diagnosis is a case in which an Automatic Test Equipment (ATE) is needed to store the huge amount of retrieved data and to drive the cyclic characteristic of the diagnosis procedure. In particular, memories diagnosis. Another interesting and blooming field is that of the mixed energy-domain devices as Micro Electro Mechanical Systems (MEMS). MEMS require unique testing apparatus applying both electrical and physical stimuli: movement, pressure, magnetic fields.

Producción bibliográfica

Artículos publicados

Arbitrados

Completo

L. M. CIGANDA

MIHST: A Hardware Technique for Embedded Microprocessor Functional On-line Self-Test. IEEE Transactions on Computers, v.: 99, 2013

Palabras clave: Built-in self-test; Microprocessors; Online test

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal

Medio de divulgación: Internet ; ISSN: 00189340 ; DOI: 10.1109/TC.2013.165

http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6579592&queryText%3Dciganda

Abstract Testing processor cores embedded in Systems-on-Chip (SoCs) is a major concern for industry nowadays. In this paper, we describe a novel solution which merges the SBST and BIST principles. The technique we propose forces the processor to execute a compact SBST-like test sequence by using a hardware module called MIcroprocessor Hardware Self-Test (MIHST) unit, which is intended to be connected to the system bus like a normal memory core, requesting no modification of the processor core internal structure. The benefit of using the MIHST approach is manifold: while guaranteeing the same or higher defect coverage of the traditional SBST approach, it reduces the time for test execution, better preserves the processor core Intellectual Property (IP), does not require the system memory to store the test program nor the test data, and can be easily adopted for non-concurrent on-line testing, since it minimizes the required system resources. The feasibility and effectiveness of the approach were evaluated on a couple of pipelined processors.

Completo

L. M. CIGANDA

An Adaptive Low-Cost Tester Architecture Supporting Embedded Memory Volume Diagnosis. IEEE Transactions on Instrumentation and Measurement, v.: 61 4, p.: 1002 - 1018, 2012

Palabras clave: Built-in self-test; embedded systems; Random access memory; IEEE 1500 wrappers; adaptive low cost tester architecture; fault diagnosis

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal

Medio de divulgación: Papel ; ISSN: 00189456 ; DOI: 10.1109/TIM.2011.2179822

http://ieeexplore.ieee.org/xpls/icp.jsp?arnumber=6146456

Abstract This paper describes the working principle and an implementation of a low-cost tester architecture supporting volume test and diagnosis of built-in self-test (BIST)-assisted embedded memory cores. The described tester architecture autonomously executes a diagnosis-oriented test program, adapting the stimuli at run-time, based on the collected test results. In order to effectively allow the tester architecture to interact with the devices under test with an acceptable time overhead, the approach exploits a special hardware module to manage the diagnostic process. Embedded static RAMs equipped with diagnostic BISTs and IEEE 1500 wrappers were selected as case study; experimental results show the feasibility of the approach when having a field-programmable gate array available on the tester and its effectiveness in terms of diagnosis time and required tester memory with respect to traditional testers executing diagnosis procedures by means of software running on the host computer.

Completo

L. M. CIGANDA

A Parallel Tester Architecture for Accelerometer and Gyroscope MEMS Calibration and Test. Journal of Electronic Testing: Theory and Applications, v.: 27 3, p.: 389 - 402, 2011

Palabras clave: MEMS testing; MEMS calibration; Accelerometer; Gyroscope; Automatic Test System

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal

Medio de divulgación: Papel ; Lugar de publicación: Springer US ; ISSN: 09238174 ; DOI: 10.1007/s10836-011-5210-2

http://link.springer.com/article/10.1007%2Fs10836-011-5210-2/fulltext.html

Abstract This paper describes a tester architecture for Accelerometer and Gyroscope Micro-ElectroMechanical System (MEMS) devices test and calibration, allowing increased parallelism rate and process accuracy. The proposed tester architecture tackles some critical issues related to MEMS testing, such as mitigating mechanical concerns that potentially impact on the equipment Mean Time Between Maintenance and guaranteeing a sufficient number of measurements in the time unit. The proposed strategy consists in an innovative and low cost tester resource partitioning that overcomes current limitations to multisite Accelerometer and Gyroscope MEMS testing. A tester prototype was implemented exploiting FPGAs; feasibility and effectiveness of the proposed methodology was demonstrated on commercial accelerometer and gyroscope MEMS devices. Topics Computer-Aided Engineering (CAD, CAE) and Design Electrical Engineering Circuits and Systems Industry Sectors IT & Software Electronics Engineering Aerospace Telecommunications Automotive

Artículos aceptados

Capitulos de Libro

Capítulo de libro publicado

Baklanova Elena; L. M. CIGANDA; JING TIAN G.; MIRZAEI P.; SANABRIA J.; WANG XUEYUN J.

E-Heels , 2013

Libro: Exercising Creativity 2012. *v.:* 1 , 1, *p.:* 57 - 66,

Organizadores: Daniel Collado-Ruiz, Hesamedin Ostad-Ahmad-Ghorabi

Editorial: Editorial Universitat Politécnica de Valéncia , Valéncia

Palabras clave: creativity; engineering

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Elecrtonica aplicada y comercializacion

Medio de divulgación: Papel; *ISSN/ISBN:* 9788490480489;

Trabajos en eventos

Completo

RIEFERT A.; L. M. CIGANDA; SAUER M.; BERNARDI P.; SONZA REORDA M.; BECKER B.

An effective approach to automatic functional processor test generation for small-delay faults , 2014

Evento: Internacional , Design, Automation and Test in Europe Conference and Exhibition (DATE) , Dresden (Germany) , 2014

Anales/Proceedings: 1 , 6Arbitrado: SI

Editorial: IEEE - INST ELECTRICAL ELECTRONICS ENGINEERS INC

Palabras clave: automatic test pattern generation; microprocessor chips; functional processor test; at-speed execution; bounded model checking; miniMIPS

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing

Medio de divulgación: CD-Rom;

Functional microprocessor test methods provide several advantages compared to DFT approaches, like reduced chip cost and at-speed execution. However, the automatic generation of functional test patterns is an open issue. In this work we present an approach for the automatic generation of functional microprocessor test sequences for small-delay faults based on Bounded Model Checking. We utilize an ATPG framework for small-delay faults in sequential, non-scan circuits and propose a method for constraining the input space for generating functional test sequences (i.e., test programs). We verify our approach by evaluating the miniMIPS microprocessor. In our experiments we were able to reach over 97 % fault efficiency. To the best of our knowledge, this is the first fully automated approach to functional microprocessor test for small-delay faults.

Completo

BERNARDI P.; L. M. CIGANDA; SONZA REORDA M.; HAMDIOUI S.

An efficient method for the test of embedded memory cores during the operational phase , 2013

Evento: Internacional , 22nd Asian Test Symposium , Yilan (Taiwan) , 2013

Anales/Proceedings: 227 , 232Arbitrado: SI

Editorial: IEEE Computer Society (USA)

Palabras clave: memory testing; system-on-chip; ad hoc module; March tests; safety critical application; software BIST

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Memory Testing

Medio de divulgación: Papel; *ISSN/ISBN:* 10817735;

System on Chip devices include an increasing number of embedded memory cores, whose test during the operational phase is often a strict requirement, especially for safety-critical applications. This paper proposes a new memory test method combining the characteristics of hardware and software solutions: the test is performed by the microcontroller/processor, while the code of the test instructions to be executed is generated on-the-fly by an ad hoc module, also in charge of checking the memory behavior. The solution is modular and does not require any modification either in the memory cores or in the processor. Moreover, it is well suited to be used for test during the operational phase. Experimental results, gathered by implementing some representative March elements and algorithms, show that the method guarantees higher defect coverage than software BIST and a test time comparable with that of traditional hardware BIST solutions with a reduced hardware cost.

Completo

L. M. CIGANDA

Automatic Generation of On-Line Test Programs through a Cooperation Scheme , 2012

Evento: Internacional , International Workshop on Microprocessor Test and Verification (MTV) , Austin TX, USA , 2012
Anales/Proceedings: IEEE Proceedings of the 13th International Workshop on Microprocessor Test and Verification (MTV) , 13 , 18Arbitrado: SI
Palabras clave: Group Evolution; System on Chip; pipelined processors; software-based self-test; on-line testing
Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal
Medio de divulgación: Internet; *ISSN/ISBN:* 9781467344418;
Abstract Test programs for Software-based Self-Test (SBST) can be exploited during the mission phase of microprocessor-based systems to periodically assess hardware integrity. However, several additional constraints must be imposed due to the coexistence of test programs with the mission application. This paper proposes a method for the generation of SBST on-line test programs for embedded RISC processors, systems where the impact of on-line constraints is significant. The proposed strategy exploits an evolutionary optimizer that is able to create a complete test set of programs relying on a new cooperative scheme. Experimental results showed high fault coverage values on two different modules of a MIPS-like processor core. These two case studies demonstrate the effectiveness of the technique and the low human effort required for its implementation.

Completo

BERNARDI P.; L. M. CIGANDA; DE CARVALHO M.; GROSSO M.; LAGOS-BENITES J.; SáNCHEZ E.; SONZA REORDA M.; BALLAN O.

On-Line Software-Based Self-Test of the Address Calculation Unit in RISC Processors , 2012

Evento: Internacional , 17th IEEE European Test Symposium (ETS) , Annecy (FR) , 2012

Anales/Proceedings: 1 , 6Arbitrado: SI

Editorial: IEEE
Palabras clave: software-based self-test; microprocessor; embedded RISC processor; on-line testing; pipelined processors; Testing

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
Medio de divulgación: Papel; *ISSN/ISBN:* 9781467306966;
Software-based Self-Test (SBST) can be used during the mission phase of microprocessor-based systems to periodically assess the hardware integrity. However, several constraints are imposed to this approach, due to the coexistence of test programs with the mission application. This paper proposes a method for the generation of SBST programs to test on-line the Address Calculation Unit of embedded RISC processors, which is one of the most heavily impacted by the online constraints. The proposed strategy achieves high stuck-at fault coverage on both a MIPS-like processor and an industrial 32-bit pipelined processor; these two case studies show the effectiveness of the technique and the low effort.

Completo

BERNARDI P.; L. M. CIGANDA; GROSSO M.; SáNCHEZ E.; SONZA REORDA M.

A SBST strategy to test microprocessors' branch target buffer , 2012

Evento: Internacional , IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS) , Tallinn (Estonia) , 2012
Anales/Proceedings: 1 , 6Arbitrado: SI

Editorial: IEEE
Palabras clave: microprocessor; software-based self-test; branch prediction; branch target buffer; pipelined microprocessor; functional testing method

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
Medio de divulgación: Papel; *ISSN/ISBN:* 9781424497546;
A Branch Target Buffer (BTB) is a mechanism to support speculative execution in order to overcome the performance penalty caused by branch instructions in pipelined microprocessors. Being an intrinsically fault tolerant unit, it is hard to achieve a good fault coverage resorting to plain functional testing methods. In this paper we analyze the causes for low functional testability and propose some techniques able to effectively face these issues. In particular, we describe a strategy to perform SBST on fully associative BTB units. The unit's general structure is analyzed, a suitable test program is proposed and the strategy to observe the test responses is explained. Feasibility and effectiveness of the proposed approach are shown on a MIPS-like processor.

Completo

BERNARDI P.; L. M. CIGANDA; SáNCHEZ E.; SONZA REORDA M.

An Effective Methodology for On-line Testing of Embedded Microprocessors , 2011

Evento: Internacional , IEEE 17th International on-line testing symposium (IOLTS) , Atene (GR) , 2011

Anales/Proceedings: 1 , 6Arbitrado: SI

Palabras clave: integrated circuit testing; microprocessor; system-on-chip; On-line test; Built-in self-test

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing

Medio de divulgación: Papel; ISSN/ISBN: 9781457710537;

Testing embedded microprocessors at mission time is nowadays a requirement in many SoC applications. In this paper, we introduce a methodology where the detection of operational faults is performed while the normal operations are temporarily suspended, by means of an ad-hoc HW module connected to the address, data and control buses of the microprocessor. This module behaves as a peripheral towards the microprocessor but is able to gain access to the bus over the system memory during the test. The proposed approach uses the microprocessor interrupt protocol to preserve the system state. Experimental results, gathered on a MIPS core, show the feasibility and effectiveness of the approach.

Completo

L. M. CIGANDA; BERNARDI P.; SONZA REORDA M.; BARBIERI D.; STRAIOTTO M.; BONARIA L.

A tester architecture suitable for MEMS calibration and testing , 2010

Evento: Internacional , International Test Conference (ITC) , Austin, TX (USA) , 2010

Anales/Proceedings: Arbitrado: SI

Editorial: IEEE

Palabras clave: micromechanical devices; MEMS calibration; MEMS testing; electrical stimuli; tester architecture

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / MEMS Testing

Medio de divulgación: Papel; *ISSN/ISBN:* 10893539/97814;

This poster outlines the working principle and an implementation of a tester architecture supporting MEMS calibration and testing; the tester works adaptively, providing electrical stimuli at run-time according to the collected results. The tester manages the calibration and testing process by means of a special hardware module, saving time and avoiding tester parallelism limitations due to massive wiring. Feasibility and effectiveness of the proposed method have been evaluated through simulations before being possibly introduced in commercial MEMS accelerometer testers.

Completo

FERNáNDEZ S.; BERGERET A.; L. M. CIGANDA; OLIVER J. P.

Diseño de placas con lógica programable como experiencia educativa en cursos de grado. , 2009

Evento: Internacional , IX Jornadas de Computación Reconfigurable y Aplicaciones , Alcalá de Henares (ES) , 2009

Anales/Proceedings: Actas de las IX jornadas de computación reconfigurable y aplicaciones , 1 , 10Arbitrado: SI

Editorial: Universidad de Alcalá

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Enseñanza

ISSN/ISBN: 9788481388329;

Completo

L. M. CIGANDA; ABATE F.; BERNARDI P.; BRUNO M.; SONZA REORDA M.

An enhanced FPGA-based low-cost tester platform exploiting effective test data compression for SoCs , 2009

Evento: Internacional , 12th International Symposium on Design and Diagnostics of Electronic Circuits & Systems , Liberec (CZ) , 2009

Anales/Proceedings: 1 , 6Arbitrado: SI

Palabras clave: design for testability; integrated circuit testing; system-on-chip; FPGA based tester; test compression / decompression; Automatic testing

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Digital Circuits Testing

Medio de divulgación: Papel; *ISSN/ISBN:* 9781424433414;

Reducing the cost of test (in particular by reducing its duration and the cost of the required ATE) is a common goal which has largely been pursued in the past, mainly by introducing suitable on chip Design for Testability (DfT) circuitry. Today, the increasing popularity of sophisticated DfT architectures and the parallel emergence of new ATE families allow the identification of innovative solutions effectively facing that goal. In this paper we face the increasingly common situation of SoCs adopting the IEEE 1149.1 and 1500 standards for the test of the internal cores, and explore the idea of storing the test program on the tester in a compressed form, and decompressing it on-the-fly during test application. This paper proposes an improved version of an data compression/decompression technique which is well suited for reducing the size of test programs stored on the tester; this technique is particularly effective for very long sequential test vectors generated to test SoCs by means of low-cost test procedures; thus, the paper outlines the characteristics of an FPGA-

based low-cost tester platform that takes advantage of the described compression schema. The effectiveness of the proposed methodology was demonstrated by practically testing some SoCs equipped with suitable DfT for supporting low-cost testing resorting to a low-cost tester implementing the proposed architecture and the compression/decompression technique.

Completo

OLIVER J. P.; FERNáNDEZ S.; HAIM F.; RODRíGUEZ J ; L. M. CIGANDA; ROLANDO, P.

Laboratorios en casa: Una Nueva Alternativa Para Cursos Masivos de Diseño Lógico Digital , 2006

Evento: Internacional , VII Congreso de Tecnologías Aplicadas a la Enseñanza de la Electrónica , Madrid (ES) , 2006

Anales/Proceedings: 1 , 7Arbitrado: SI

Palabras clave: Enseñanza; Diseño digital; laboratorio@home

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Enseñanza

Medio de divulgación: Papel; *ISSN/ISBN:* 9788468995908;

Completo

HAIM F.; FERNáNDEZ S.; RODRíGUEZ J ; L. M. CIGANDA; ROLANDO, P.; OLIVER J. P.

Laboratory at Home: Actual Circuit Design and Testing Experiences in Massive Digital Design Courses , 2006

Evento: Internacional , 9th International Conference on Engineering Education , San Juan (PR) , 2006

Anales/Proceedings: 5 , 9Arbitrado: SI

Palabras clave: computer aided instruction; distance learning; electronic engineering education; logic design; hardware kits; lab at home

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Education

Medio de divulgación: Papel;

An innovative laboratory methodology for thedigital design introductory course is presented. We replacethe traditional lab experiences, where students have tocome to school classrooms, with a “lab at home” concept.More than 65 kits with a programmable logic board aregiven to groups of students for the whole semester. Thus,students perform all the lab stages, including analyzing theproblems, designing a solution and testing the actualcircuit, at their homes. Then, they come to school to showtheir circuits to the professors. These evaluation instances,together with a final exam, are enough to adequatelyevaluate the students’ work, eliminating the need of a mid-term exam. This is the third edition of the course with thismethodology. A survey of opinion showed that theexperience was very successful among students. Moreover,it is very suitable for massive courses and easily scalable,providing actual hardware platforms for students at anaffordable cost for the institution.

Evaluaciones

Evaluación de Publicaciones

2014 / 2014

Nombre: Very Large Scale Integration of System-on-Chip (VLSI-SoC),

Cantidad: Menos de 5

Evaluación de Publicaciones

2014 / 2014

Nombre: Journal of Electronic Testing: Theory and Applications,

Cantidad: Menos de 5

Review of manuscript: 'VHDL Modelling of Full Fault Detection Coverage Memory Tester'

Formación de RRHH

Tutorías concluidas

Posgrado

Tesis de maestría

Implementation and Testing of a Parametric Branch Prediction Unit in Pipelined Processors , 2012

Tipo de orientación: Cotutor o Asesor

Nombre del orientado: FU Mengyang

Politecnico di Torino , Italia , Electronic Engineering

Palabras clave: Testing of processors; branch prediction; branch target buffer; software-based self-test
Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
Medio de divulgación: Papel, *Pais/Idioma:* Italia/Inglés
Información adicional: Branch instructions can possibly reduce the performance of pipelined processors by interrupting the steady instruction flow into the pipeline. In past decades, several strategies have been developed to solve this problem. Among them, Branch Target Buffer (BTB) is a method which uses a small associated memory to store the information of several executed branches. The prediction based on these information will significantly improve the performance of pipelined processors. However, this kind of prediction units brings difficulties on testing due to their deeply embedded architectures. This thesis proposes a design of a parametric branch prediction unit using a BTB with 2-bit predictor in pipelined processors. Then in order to test such prediction units, Software Based Self-Test (SBST) method is introduced. Adopting this method, suitable test strategies are proposed considering the structure of the BTB and the test programs for the prediction unit are developed and explained based on a processor core with MIPS architecture. This method used is effective and cost-economical on testing such prediction units. Moreover, both of the proposed design and testing approaches could be transplanted to other MIPS-like processors with a limited effort.

Otros datos relevantes

Jurado/Integrante de comisiones evaluadoras de trabajos académicos

Tesis

Candidato: Cosenza,Domingo,Fu,Gullo,Pasturenzi,Rosato,Sandiano,Vasciave

BENSO A.; BERNARDI P.; L. CIGANDA; DI CARLO S.; MORISIO M.; SáNCHEZ E.; SQUILLERO G.

Commissioni per gli Esami di Laurea della Sessione del mese di novembre 2012, dei corsi di studio afferenti al Collegio di Ingegneria Informatica, del Cinema e Meccatronica. , 2012

Tesis (Computer Engineering) - Politecnico di Torino - Italia

Referencias adicionales: Italia , Inglés
Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería de Sistemas y Comunicaciones / Education

Presentaciones en eventos

Congreso

A tester architecture suitable for MEMS calibration and testing , 2010

Tipo de participación: Poster, *Carga horaria:* 40
Referencias adicionales: Estados Unidos; *Nombre del evento:* International Test Conference; *Nombre de la institución promotora:* IEEE

Palabras clave: MEMS calibration; MEMS testing; Automatic Test Equipment; FPGA based tester; test compression / decompression; parallel testing
Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / MEMS Testing

This poster outlines the working principle and an implementation of a tester architecture supporting MEMS calibration and testing; the tester works adaptively, providing electrical stimuli at run-time according to the collected results. The tester manages the calibration and testing process by means of a special hardware module, saving time and avoiding tester parallelism limitations due to massive wiring. Feasibility and effectiveness of the proposed method have been evaluated through simulations before being possibly introduced in commercial MEMS accelerometer testers.

Simposio

A SBST strategy to test microprocessors' branch target buffer , 2012

Tipo de participación: Expositor oral, *Carga horaria:* 24
Referencias adicionales: Estonia; *Nombre del evento:* 15th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems; *Nombre de la institución promotora:* IEEE
Palabras clave: software-based self-test; microprocessor; functional testing method; branch target buffer; Branch prediction unit; test program
Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
A Branch Target Buffer (BTB) is a mechanism to support speculative execution in order to overcome the performance penalty caused by branch instructions in pipelined microprocessors. Being an intrinsically fault tolerant unit, it is hard to achieve a good fault coverage resorting to plain functional testing methods. In this paper we analyze the causes for low functional testability and propose some techniques able to effectively face these issues. In particular, we describe a strategy to perform SBST on fully associative BTB units. The unit's general structure is analyzed, a suitable test program is proposed and the strategy to observe the test responses is explained. Feasibility and effectiveness of the proposed approach are shown on a MIPS-like processor.

Simposio

An Effective Methodology for On-line Testing of Embedded Microprocessors , 2011

Tipo de participación: Expositor oral, *Carga horaria:* 24

Referencias adicionales: Grecia; *Nombre del evento:* 17th IEEE International On-Line Testing Symposium; *Nombre de la institución promotora:* IEEE

Palabras clave: microprocessor; On-line test; system-on-chip; ad hoc hardware module; Built-in self-test

Areas del conocimiento: Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing

Testing embedded microprocessors at mission time is nowadays a requirement in many SoC applications. In this paper, we introduce a methodology where the detection of operational faults is performed while the normal operations are temporarily suspended, by means of an ad-hoc HW module connected to the address, data and control buses of the microprocessor. This module behaves as a peripheral towards the microprocessor but is able to gain access to the bus over the system memory during the test. The proposed approach uses the microprocessor interrupt protocol to preserve the system state. Experimental results, gathered on a MIPS core, show the feasibility and effectiveness of the approach.

Indicadores de producción

Producción bibliográfica	*15*
Artículos publicados en revistas científicas	*3*
Completo (Arbitrada)	3
Artículos aceptados para publicación en revistas científicas	*0*
Trabajos en eventos	*11*
Completo (Arbitrada)	11
Libros y capítulos de libros publicados	*1*
Capítulo de libro publicado	1
Textos en periódicos	*0*
Documentos de trabajo	*0*
Producción técnica	*0*
Productos tecnológicos	*0*
Procesos o técnicas	*0*
Trabajos técnicos	*0*
Otros tipos	*0*
Evaluaciones	*2*
Evaluación de Publicaciones	2
Formación de RRHH	*1*
Tutorías/Orientaciones/Supervisiones concluidas	*1*
Tesis de maestría	1
Tutorías/Orientaciones/Supervisiones en marcha	*0*

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